a first transistor formed on a first region of the substrate and including a first gate electrode arranged along a first direction; and

a second transistor formed on a second region of the substrate and including a second gate electrode arranged along the first direction,

wherein a side wall of said first gate electrode at one end of a channel direction is connected to a side wall of said second gate electrode at one end of the channel direction.

C1 cont'd

28. (Twice Amended) A device according to claim 27, wherein a part of the side wall of the first gate electrode is only connected to a part of the side wall of the second gate electrode and said part of the side wall of the first gate electrode and said part of the side wall of the second gate electrode are substantially perpendicular to a surface of said semiconductor substrate.

31. (Twice Amended) A device according to claim 27, wherein said first transistor includes a first insulator film, said second transistor includes a second insulator film, said first insulator film is thinner than said second insulator film, said first transistor is included in a logic circuit, and said second transistor is included in a memory cell.

C2

32. (Twice Amended) A device according to claim 27, wherein top surfaces of said first and second gate electrodes and a connection layer are coplanar.

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